

Organisational information

For registration please use the registration form which is available on the ECPE web page: www.ecpe.org
> ECPE Events > ECPE Tutorial: Power Circuits for Clean Switching Low Losses > Registration Form

www.ecpe.org/ecpe-events

Deadline for registration:

- **2 November 2017**

Participation fee:

- **€ 350,-** * for industry
- **€ 250,-** * for universities/institutes
- **€ 120,-** * for students/PhD students
(copy of student ID requested)
(limited number only)

* plus VAT

- The participation fee includes lunch, coffee/soft drinks and handouts.
- With the confirmation of registration by email you are registered for the workshop and the invoice will be sent by post.
- 50 % discount for each participant from ECPE Member Companies.
- Further information (hotel list and maps) will be provided after registration and is available on the ECPE web page.
- In case of cancellation later than two weeks before beginning or non-attendance 50 % of the participation fee is payable.
- The number of participants is limited to 35 attendees.

Organisational information

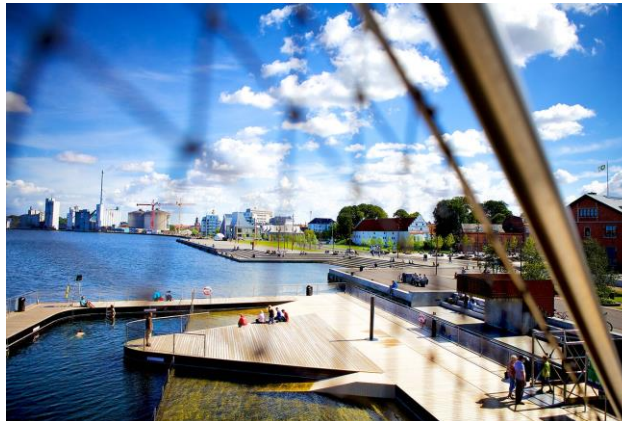
Organiser ECPE e.V.
90443 Nuremberg, Germany
www.ecpe.org

Course instructor Dr. Reinhold Bayerer,
Infineon Technologies AG

Organisation Ingrid Bollens, ECPE e.V.
+49 (0)911 / 81 02 88 – 10
Ingrid.bollens@ecpe.org

Venue Aalborg University
Department of Energy Technology
Pontoppidanstraede 111
DK-9220 Aalborg
Denmark

Graph Copyright by Infineon



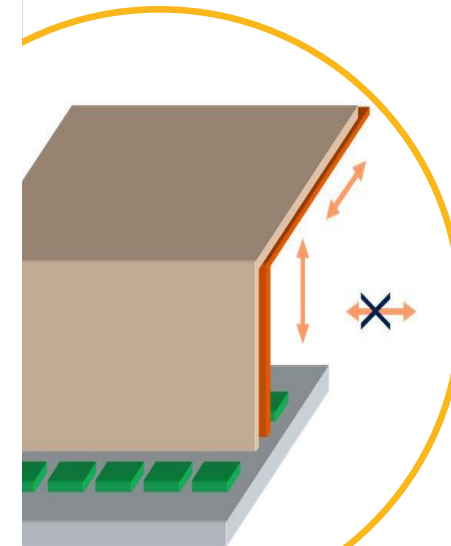
Further information (hotel list and maps) will be provided after registration.



ECPE Tutorial

Power Circuits for Clean Switching and Low Losses

9 November 2017
Aalborg University
Aalborg, Denmark



Hosted by 

DEPARTMENT OF ENERGY TECHNOLOGY
AALBORG UNIVERSITY

ECPE Tutorial

Power Circuits for Clean Switching and Low Losses

9 November 2017
Aalborg, Denmark

This tutorial will teach the various effects of parasitic inductance (L_s) in power electronics. As power density and current density is continuously rising, parasitic inductance and resistance become more and more the limiting factors. The problem is the product inductance times current ($L_s \cdot I$) rising, simultaneously, if designs do not improve.

Not only overvoltage during switching is the problem but for bipolar power semiconductors like IGBTs and freewheeling diodes, parasitic inductance causes disadvantageous current waveforms.

In systems which have snubber capacitors additional to the DC-link capacitor and parasitic inductance in between, oscillations between these capacitors occur.

When considering power semiconductors in parallel the current sharing of controlled devices like IGBT, MOSFET and JFET can be affected by the presence of small parasitic inductance.

Parasitic inductance in the control circuit (gate circuit) decouples driver and the gates of the devices leading to increased short circuit current, for example.

To introduce these topics the tutorial will start with the basics of switching inductive loads and discussion of related waveforms. Investigations on the different effects will follow. The discussion of paralleling will be accompanied by case studies. Geometries of conductors and system design for low parasitic inductance and good current sharing will be another main part and the conclusions will summarize the benefits of related system design – clean switching and low losses.

Course instructor is Dr. Reinhold Bayerer, Infineon Technologies AG, Germany.

All presentations and discussions will be in English language.

Programme

Thursday, 9 November 2017

8:30 Start of Registration

9:00 Welcome,
T. Harder, ECPE e.V.
F. Blaabjerg, Aalborg University

Technical Presentations given by R. Bayerer, Infineon

9:15 Power Semiconductors Switching under Inductive Load

9:55 Geometry of Conductors and their Inductance – Determination and Evaluation

10:45 Coffee Break

11:00 Parasitic Inductance – Effecting Switching Characteristics and Stress Factors of Power Semiconductors

11:35 Power Devices Parasitic Inductance – Effecting Current Sharing of Paralleled Power Devices

12:15 Lunch

13:15 Case Study I:
Asymmetric Paralleling and Discussion

13:45 Case Study II:
Asymmetric Paralleling and Discussion

14:15 Parasitic Inductance – Effecting System Losses

14:35 Coffee Break

Programme

Thursday, 9 November 2017

15:00 Oscillations in DC-Bus

15:35 Parasitic Inductance meets Parasitic Resistance

15:55 Gate Inductance

16:35 Measuring Challenges and Solutions

16:55 Benefit of Circuits with Low Parasitic Inductance

17:15 Optional: Lab tour at Aalborg University

18:00 End of Tutorial